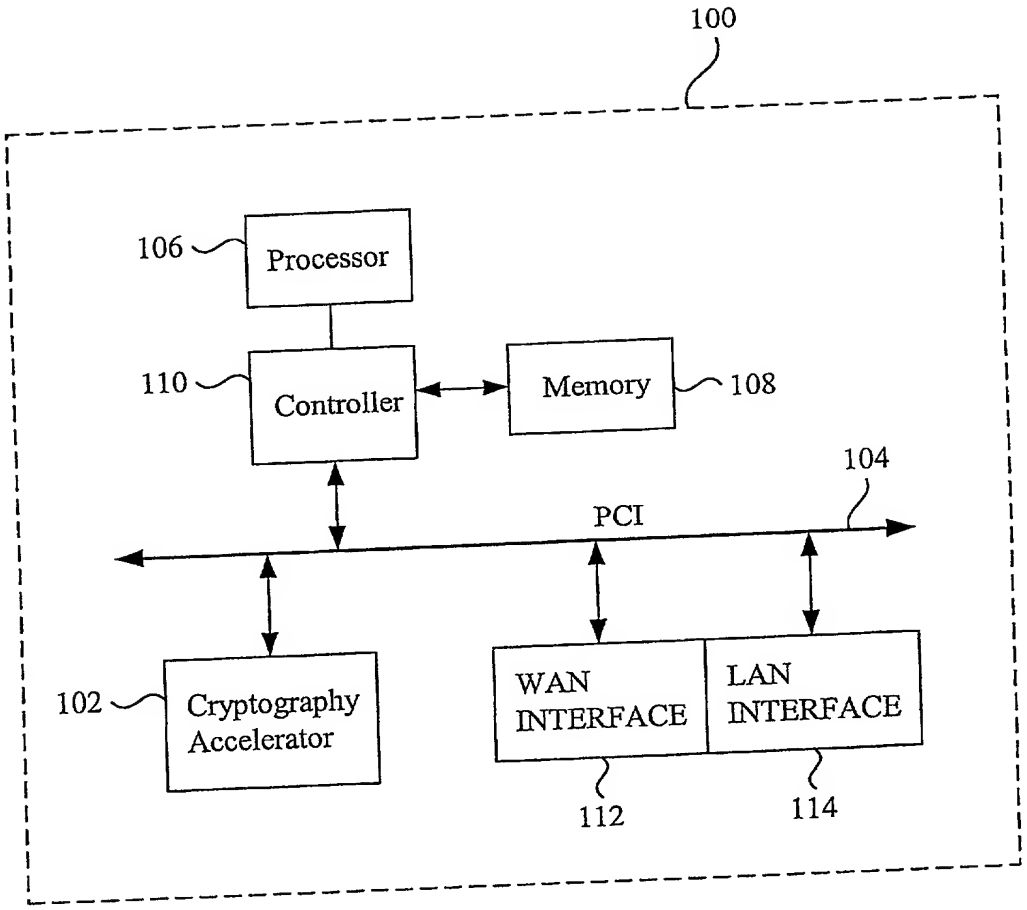

100
106
Processor
110
Controller
Memory
108
104
PCI
102
Cryptography Accelerator
WAN INTERFACE
LAN INTERFACE
112
114

FIG. 1

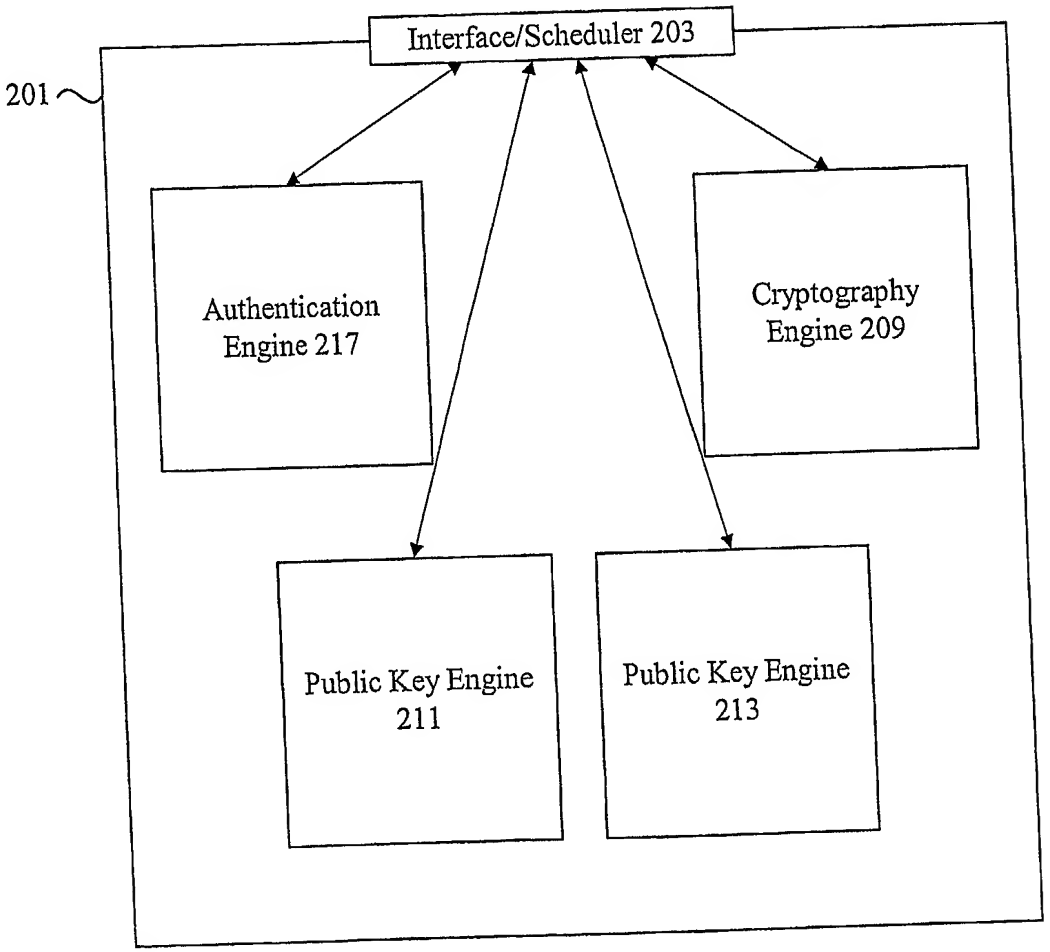


FIG. 2

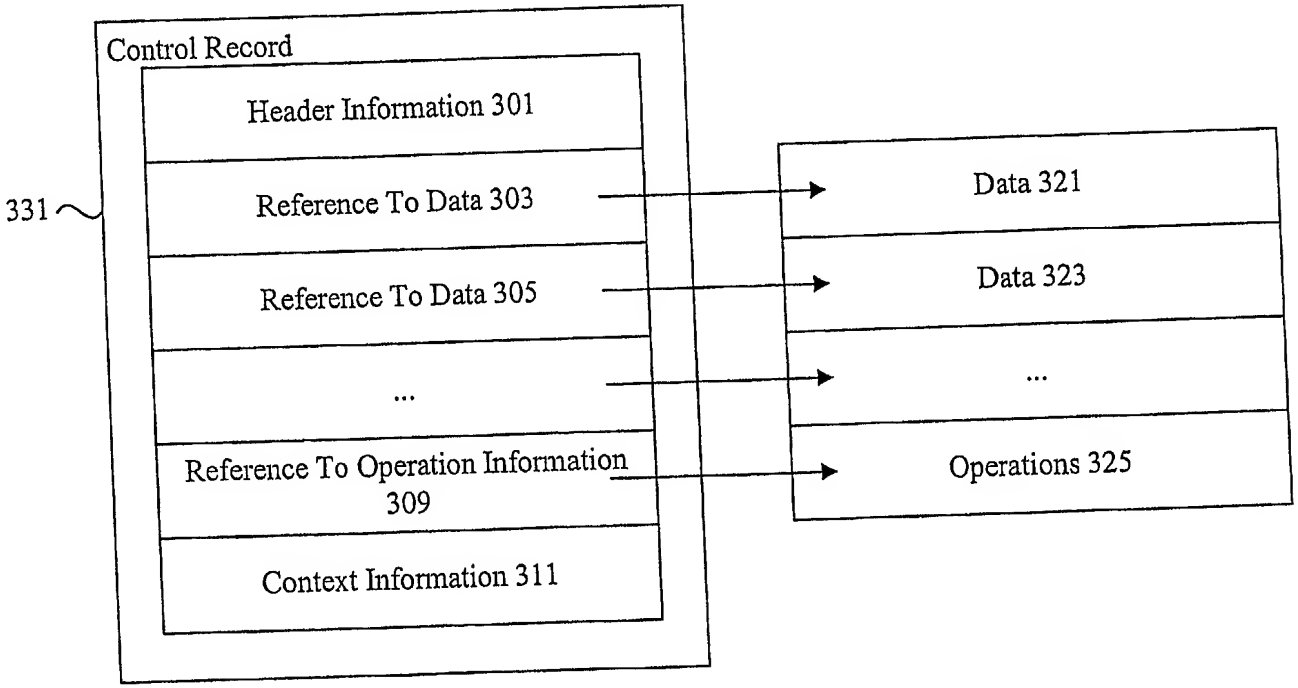

Control Record
Header Information 301
Reference To Data 303
Reference To Data 305
...
Reference To Operation Information 309
Context Information 311
331
Data 321
Data 323
...
Operations 325

FIG. 3

Host Memory 401

Block 403	Block 413	Block 423	Block 433	Block 443
Data 405	Data 415	Data 425	Data 435	Data 445
Status Bit 407	Status Bit 417	Status Bit 427	Status Bit 437	Status Bit 447

FIG. 4

Fig. 5A

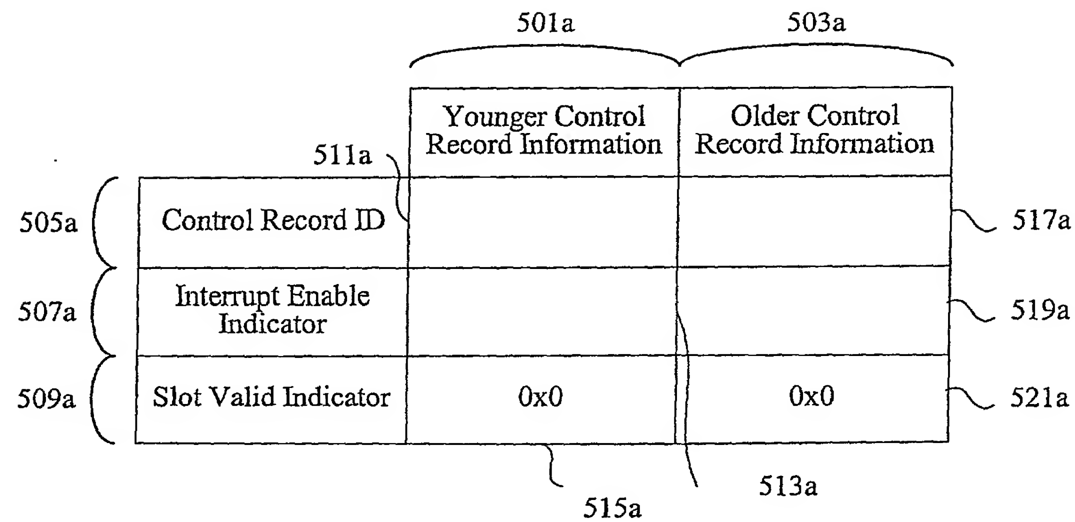


Fig. 5B

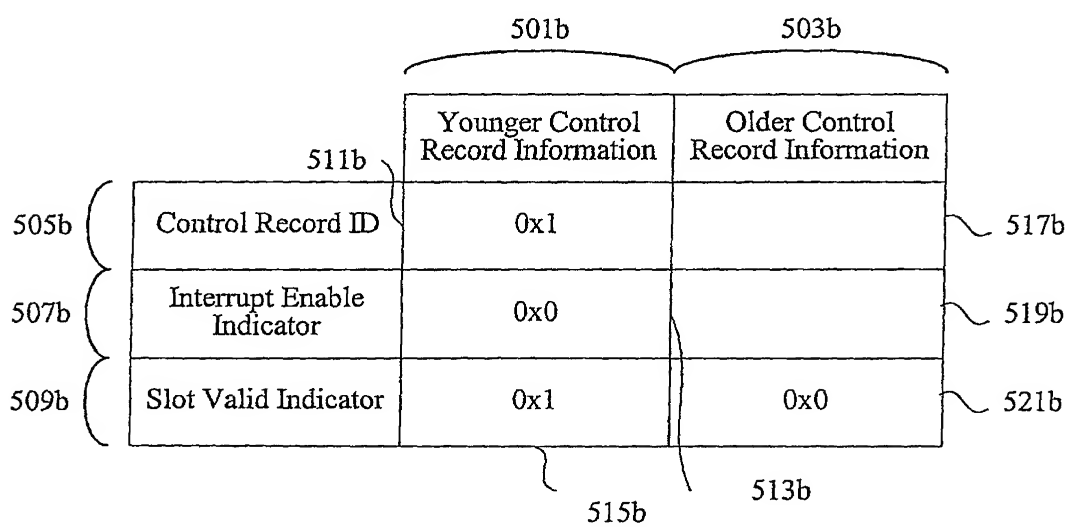


Fig. 5C

		501c	503c	
	511c	Younger Control Record Information	Older Control Record Information	
505c	Control Record ID	0x0	0x1	517c
507c	Interrupt Enable Indicator	0x1	0x0	519c
509c	Slot Valid Indicator	0x1	0x1	521c
		515c	513c	

Fig. 5D

		501d	503d	
	511d	Younger Control Record Information	Older Control Record Information	
505d	Control Record ID		0x1	517d
507d	Interrupt Enable Indicator		0x1	519d
509d	Slot Valid Indicator	0x0	0x1	521d
		515d	513d	

Fig. 6

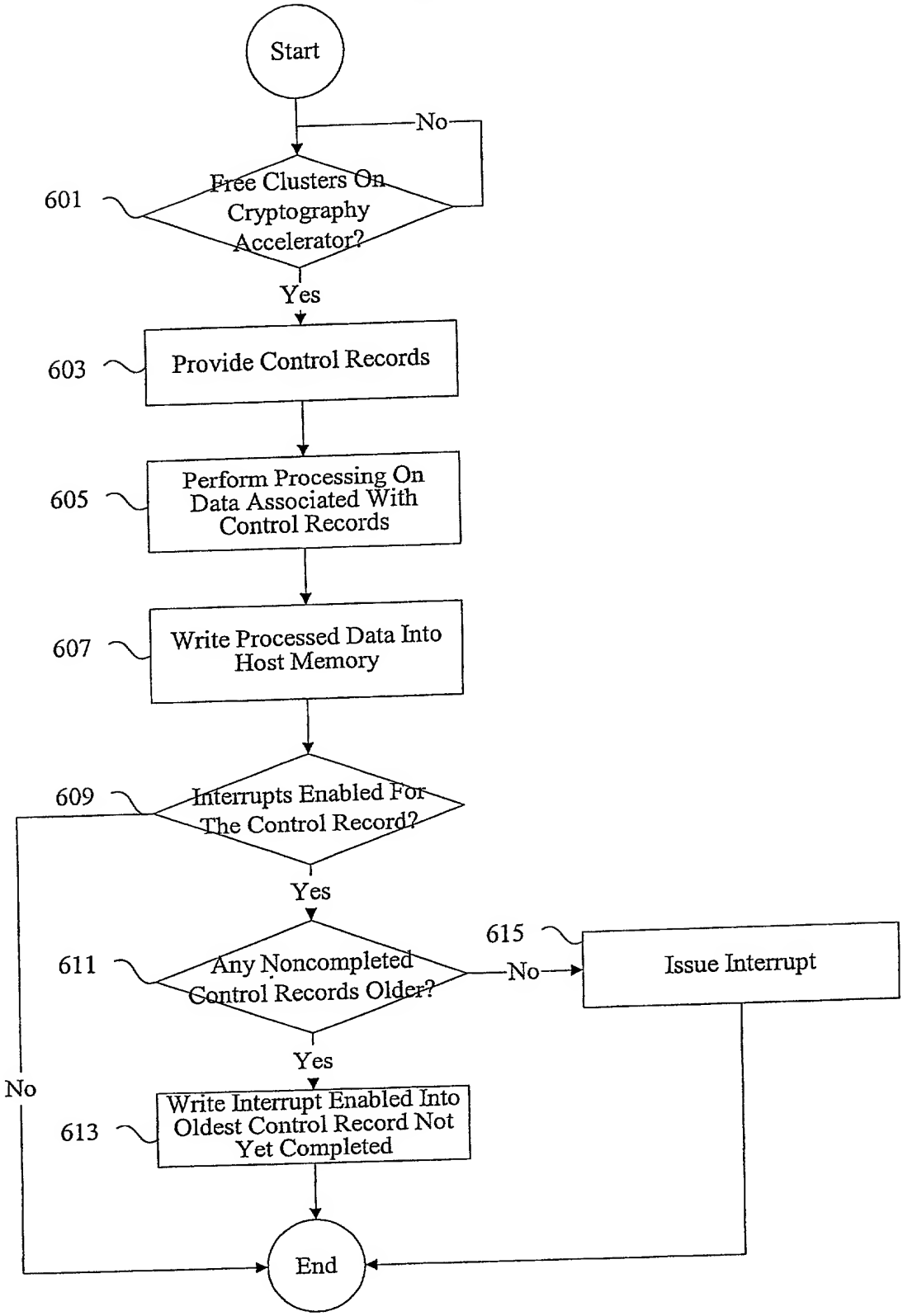
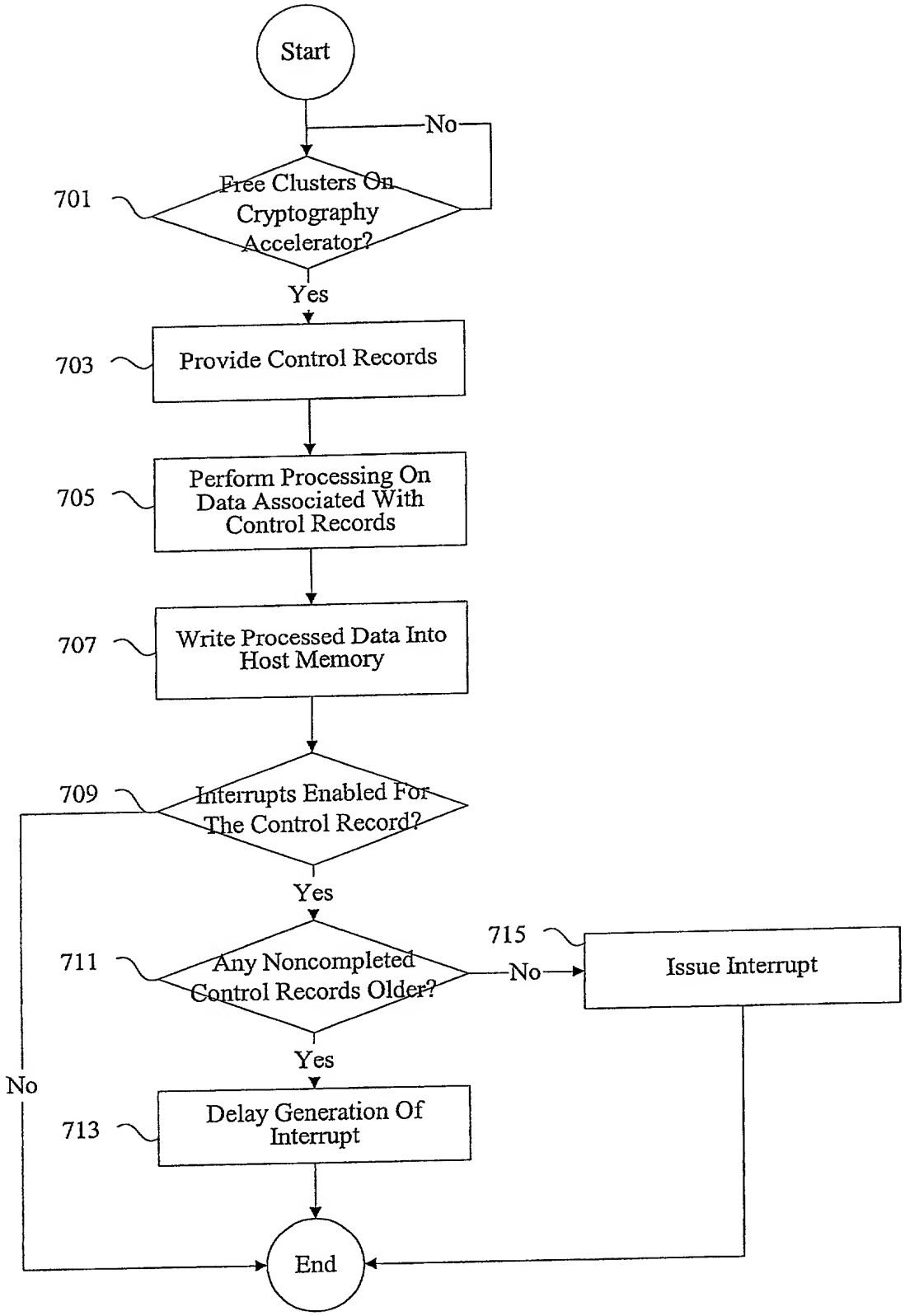

Start
No
601
Free Clusters On Cryptography Accelerator?
Yes
603
Provide Control Records
605
Perform Processing On Data Associated With Control Records
607
Write Processed Data Into Host Memory
609
Interrupts Enabled For The Control Record?
Yes
611
Any Noncompleted Control Records Older?
615
No
Issue Interrupt
Yes
No
613
Write Interrupt Enabled Into Oldest Control Record Not Yet Completed
End

Fig. 7


Start
No
701
Free Clusters On Cryptography Accelerator?
Yes
703
Provide Control Records
705
Perform Processing On Data Associated With Control Records
707
Write Processed Data Into Host Memory
709
Interrupts Enabled For The Control Record?
Yes
711
Any Noncompleted Control Records Older?
715
No
Issue Interrupt
Yes
No
713
Delay Generation Of Interrupt
End